Introduction

With advancements being made at a furious pace in the field of networking, applications have started focusing on achieving the most out of the existing infrastructure. Power over Ethernet (PoE) is one such classic example that integrates power and data lines. PoE consists of two power entities: Power Sourcing Equipment (PSE) and Powered Devices (PDs), for use with the physical layers. These utilize the same LAN cabling (CAT-5 cables), that are used for transmission of data, over spare twisted pair cables. Typical applications include IP phones, WLAN access points, security cameras and RFID tag readers, to name a few.

Scope

This document focuses on Intersil's solution for the Powered Device portion of the circuit, which complies with IEEE 802.3af, the standard for PoE. An inexpensive approach with discrete circuitry has been adopted instead of an integrated solution. With PoE soon turning into a commodity market, low cost will be key, as compared to utilization of sophisticated integrated solutions. The following solution has been optimized for performance per the IEEE 802.3af standard, with low cost and optimal performance as the prime objectives. The evaluation board is currently available.

Powered Device (PD)

The PD needs to be able to operate with a maximum average input power of 12.95W, and should be operational between 36V and 57V DC. Class 0 (default) was selected for this design, to provide the end user with maximum flexibility with their output power requirements. Discrete classification circuit may be added, as required, at a very low additional cost. Other specifications selected are in line with the requirements as specified in Table 33-12 of IEEE802.3af, and are listed below:

Specifications Chosen for the PD Design

Operating Input Voltage range: 36V-57V DC

Max. Input Operating Current: 350mA

Max. Input Inrush Current: 400mA

Output Voltage: 3.3V

Output Current: 3.35A

Ripple: $50mV_{P-P}$

Typical Efficiency: 87%

Isolation: 1500V DC

Selection of the Power Topology

While selecting the topology for this application, the emphasis was placed on two key features: optimized performance and low cost. A simple low-power design requirement, combined with low cost target dictated the use of a flyback converter for this application. Given that the input power available is limited by the PSE, high efficiency becomes an essential requirement. The converter is being operated in the continuous current mode to achieve this goal.

IC Selection

Intersil's superior industry-standard ISL684x family of PWM controllers would best serve the needs of this design. Some key features of this family of parts include:

- Tight internal voltage reference of 1% over temperature.
- 40ns peak current sensing.
- 1A MOSFET driver

ISL6844 was selected for its large UVLO hysteresis, UVLO start threshold, and the fact that the converter has been designed for a maximum operational duty cycle of 50%, thus protecting the IC by limiting the duty cycle in case of extreme fault conditions.

Transformer Design

The design of the flyback transformer is an iterative process, and involves the following steps:

- Calculate the energy storage needed.
- Select core geometry and material.
- Select the maximum desired flux density of operation.
- Select core size.
- Calculate the maximum flux density.
- Calculate the turns ratio.
- Select the wire gauge, number of strands, winding order and insulation requirements.
- Estimate the losses.
- Verify the design.

While the details of the design are not discussed in this document, as a summary, it was decided to proceed with an EP-13 core, in order to achieve a balance of good performance and low cost. The evaluation board provides the end users with the option of using two other low-profile cores for their transformer design, and can be tailored to meet the customers' specific requirements.

Primary MOSFET Selection

The primary MOSFET needs to be able to handle the peak voltage stress on the primary of a flyback design, given by:

$$V_{DSFETprimary} = V_{DSFETprimary} + [N_{ps} \times (V_{out} + V_f)] = 57 + [6 \times (3.3 + 0.4)] = 79.2V \quad \text{(EQ. 1)}$$

where

N_{ps} = Turns ratio between the primary and the secondary windings

V_{out} = Output Voltage

V_f = Forward drop across the diode (negligible in the case of synchronous rectification)

As a good design practice, some margin is provided to this peak stress voltage to accommodate transient spikes and for a good reliable performance over time. Providing a 30% design margin as a rule of thumb, the minimum rating on the primary MOSFET needs to be 103V. HAT2088R-EL-E, a 200V part, was selected for the purpose, taking into account also that this part has a very low capacitance and a very low gate charge, key to keep the power losses to a minimum.

Rectification

Two versions of the evaluation board are available:

- A synchronous rectified output, with the converter operating in the continuous current mode, to attain the high efficiency target. This version is available as ISL6844EVAL1Z. For this implementation, a discrete gate drive circuit was designed, using a gate drive transformer to meet isolation requirements.
- A conventionally rectified version, ISL6844EVAL2Z, is also available for end users to whom tight regulation is not critical, but emphasis is on cost saving at the expense of slightly reduced efficiency. Since the feedback is tapped off the primary auxiliary winding in this application, the varying diode drop with load results in slightly lower regulation. In the case of a synchronous rectified output, the drop across the switching device is negligible. The conventionally rectified version also operates in the continuous current mode to maximize efficiency, and lower the output ripple.

Secondary MOSFET Selection

The secondary MOSFET selection follows slightly different criteria. The emphasis here is more to reduce the DC losses, and hence a very low $r_{DS(ON)}$ device is required. At the same time, care needs to be taken to ensure that the gate charge required to drive the FET is not too large, as this may need a beefy gate drive circuit. The peak voltage will be seen at minimum duty cycle (maximum input voltage). The minimum and maximum duty cycle can be calculated by:

$$D_{min} = \frac{\left(\frac{V_{out}}{V_{inmax}} \times N_{ps}\right)}{\left[1 + \left(\frac{V_{out}}{V_{inmax}} \times N_{ps}\right)\right]} = \frac{\left(\frac{3.3}{57} \times 6\right)}{\left[1 + \left(\frac{3.3}{57} \times 6\right)\right]} = 0.2578 \quad \text{(EQ. 2)}$$

$$D_{max} = \frac{\left(\frac{V_{out}}{V_{inmin}} \times N_{ps}\right)}{\left[1 + \left(\frac{V_{out}}{V_{inmin}} \times N_{ps}\right)\right]} = \frac{\left(\frac{3.3}{36} \times 6\right)}{\left[1 + \left(\frac{3.3}{36} \times 6\right)\right]} = 0.355 \quad \text{(EQ. 3)}$$

The peak voltage can then be calculated by:

$$V_{DSFETsecondary} = \frac{V_{out}}{D_{min}} = \frac{3.3}{0.2578} = 12.8V \quad \text{(EQ. 4)}$$

Providing a 30% design margin on similar grounds to the primary FET selection, the minimum rating on the secondary MOSFET is about 17V. To achieve the right balance between the low $r_{DS(ON)}$, to minimize conduction losses, and low Q_g, to minimize switching losses, HAT2168H-EL-E, a 30V device was chosen.

Output Filter

The output capacitance needs to meet the ripple and noise requirements, and also be able to handle the ripple current. The peak secondary current can be approximately calculated using the formula given in EQ. 5 below:

$$Isp = \left(\frac{V_{out} \times I_{out}}{V_{inmin} \times \eta} \times \frac{1}{D_{max}} \times N_{ps}\right) + \left(\frac{V_{inmin} \times D_{max}}{L \times fsw} \times \frac{1}{2}\right) = \left(\frac{3.3 \times 3.35}{36 \times 0.87} \times \frac{1}{0.355} \times 6\right) + \left(\frac{36 \times 0.355}{155 \times 10^{-6} \times 200 \times 10^{3}} \times \frac{1}{2}\right) = 6.2A \quad \text{(EQ. 5)}$$

where

I_{sp} = Peak Secondary Current

I_{sp} = Efficiency of the Converter

f_{sw} = Switching Frequency of the Converter

L = Magnetizing Inductance of the Transformer

The ripple current handling capacity of the output capacitor needs to be at least 2.85A at full load, the ripple being the difference between the peak current and the maximum DC load seen. To bring the voltage ripple down to less than $100mV_{P-P}$, the maximum ESR of the capacitor can be calculated from EQ. 6below:

$$ESR \leq \frac{VoltageRipple}{PeakCurrent - FullLoadCurrent} = \frac{50mV}{6.2 - 3.35} = 17.54m\Omega \quad \text{(EQ. 6)}$$

A POSCAP was selected, to provide for variations in ripple current and ESR over temperature, as also to account for parasitic elements. A 10µF ceramic capacitor was added to share the stress on the filter capacitor. Design margin has been provided to account for noise spikes.

Feedback Network

The feedback is being tapped off the primary auxiliary winding. This is one of the advantages of selecting the flyback topology, since the auxiliary winding voltage follows the output. This scheme was fully exploited, since the load fluctuation is minimal, and that load regulation does not suffer much at these power levels (Load Regulation is shown in Figure 6). For tighter regulation requirements, an opto-coupled solution would need to be used, at the expense of additional cost.

Additional Features

The Evaluation Board has the option of either directly plugging into an ethernet jack, or using an external power supply to provide the input power. It provides an additional bridge-rectification circuit, and a diode that offers reverse polarity protection in case the bridge-rectification is not used. It also provides the user with the option of using a 10/100 Base (T3) or a Gigabit Network Ethernet Transformer (T4), based on the end application. For convenience, the Gigabit Network Ethernet Transformer is included as part of the Evaluation Kit, but is not populated on the board. For users with a Gigabit Network requirement, T4 will have to be populated on the board, and T3 removed.

Typical Performance Characteristics

Typical performance waveforms are shown below, based on measurements made on an ISL6844EVAL1Z Board.

Figure 1 shows a plot of efficiencies at different input voltages. Based on these results, the efficiency target of 87% at typical loads was achieved.

Figure 2 and Figure 3 show the primary and secondary gate drive signals that drive the respective FETs.

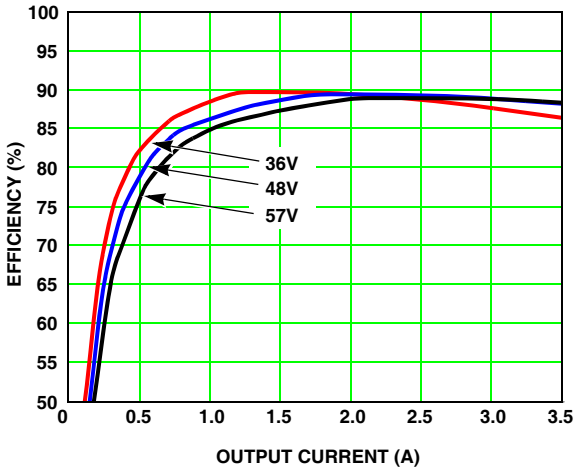


FIGURE 1. TYPICAL EFFICIENCY

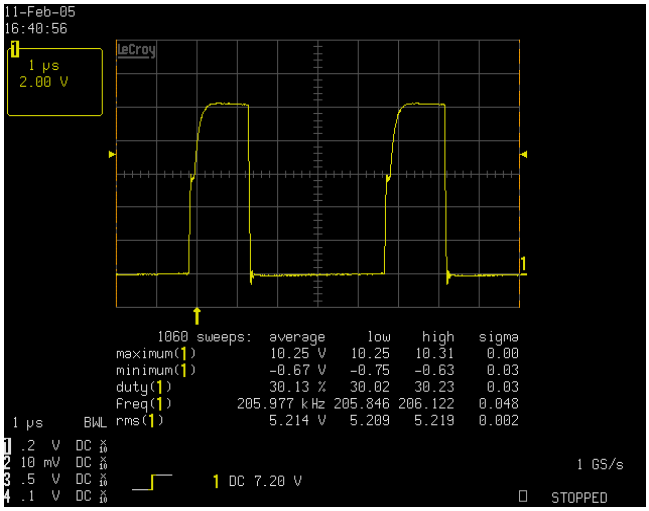


FIGURE 2. PRIMARY GATE DRIVE - Vgs of Q2
CONDITION: V_{IN} = 48V, I_{OUT} = 3.3A

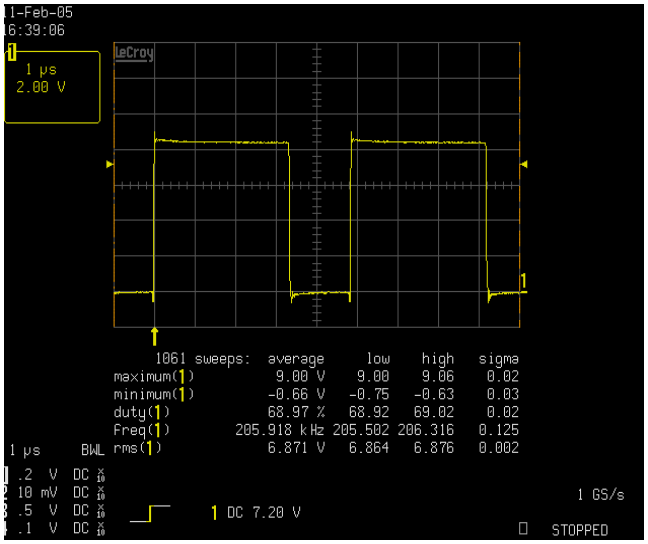
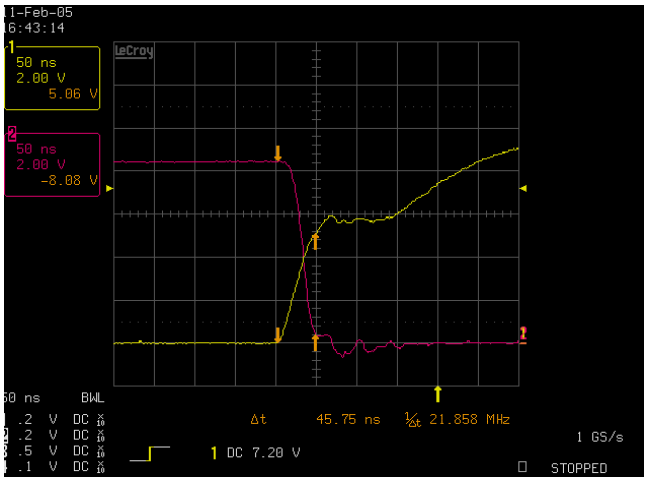


FIGURE 3. SECONDARY GATE DRIVE - Vgs OF Q3
CONDITION: V_{IN} = 48V, I_{OUT} = 3.3A



NOTE:
Channel 1: Vgs of Primary MOSFET
Channel 2: Vgs of Secondary MOSFET

FIGURE 4. GATE DRIVE TRANSITION - Q3 TO Q2
CONDITION: V_{IN} = 48V, I_{OUT} = 3.3A

The rise time of the primary FET has been deliberately reduced via a 100Ω resistor (R5), in order to ensure that the cross-conduction is minimized between the 2 switching devices. Diode CR3 has been added anti-parallel to R5 to ensure quick turn-off of the device. The cross-conduction between the 2 FETs are shown in Figure 4.

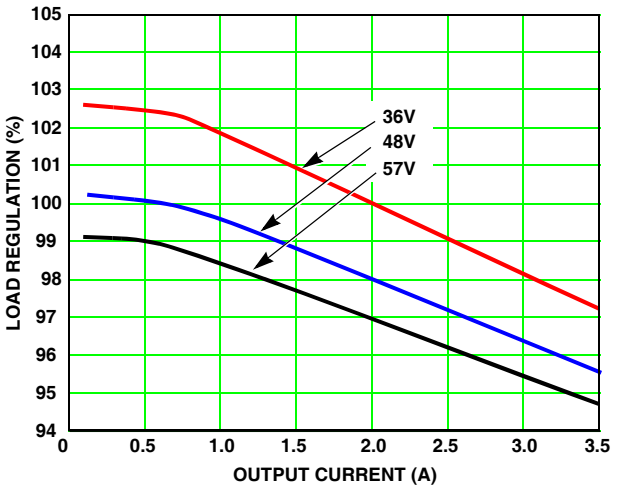


FIGURE 5. LOAD REGULATION

Load regulation of the converter for different inputs is shown in Figure 5. To shift the output voltage level, the feedback resistor R9 may be tweaked as required.

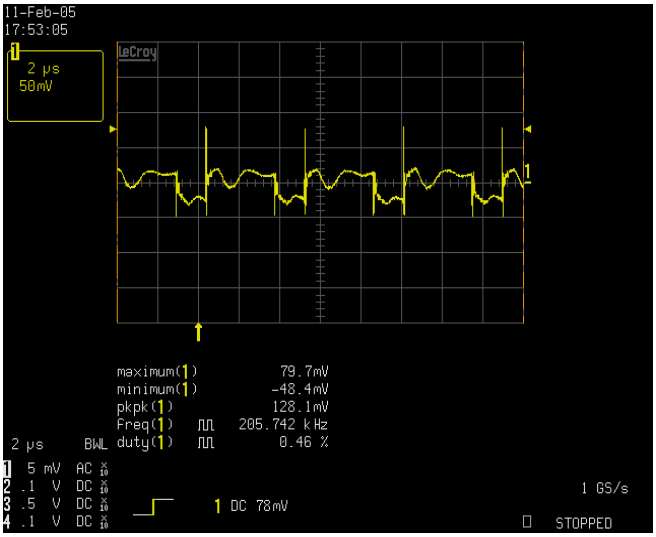


FIGURE 6. OUTPUT RIPPLE AND NOISE - 20MHz BW
CONDITION: V_{IN} = 48V, I_{OUT} = 3.3A

Output voltage ripple and noise measurements are shown in Figure 6, at a nominal input of 48V, with a load of 3.4A. Short ground leads were utilized in the measurement.

Efficiency

With a maximum available average input power of 12.95W, efficiency becomes a key parameter to consider. At these low power levels, even a few tens of milliwatts of power loss would lower the efficiency. The following is a summary of the approximate losses:

Power Transformer - 900mW

Primary FET - 100mW

Secondary Switch (FET in ISL6844EVAL1Z) - 100mW

Current Sense Resistor - 200mW

Fixed Control (Bias, Gate Drive) - 300mW

giving a total loss of about 1.6W (or 12.3%). This allows the solution to hit the 87% efficiency target.

In the case of a diode-rectified circuit (ISL6844EVAL2Z), the VI loss across the diode would be about 1W, resulting in an additional 7% power consumption. The advantage of this version is the cost savings achieved by not having to use the relatively expensive gate drive circuitry.

ISL6844EVAL2Z Performance and Differences

The major differences in performance of the conventionally rectified design versus the synchronous rectified solution have been highlighted in earlier paragraphs. The performance variations are shown below:

Figure 7 shows the efficiencies of the ISL6844EVAL2Z board with and without an additional pre-load resistor. The additional load is necessary to ensure regulation even at light loads (0.35W). The board can be used without the pre-load resistor if the minimum load seen by the system is greater than 0.2A.

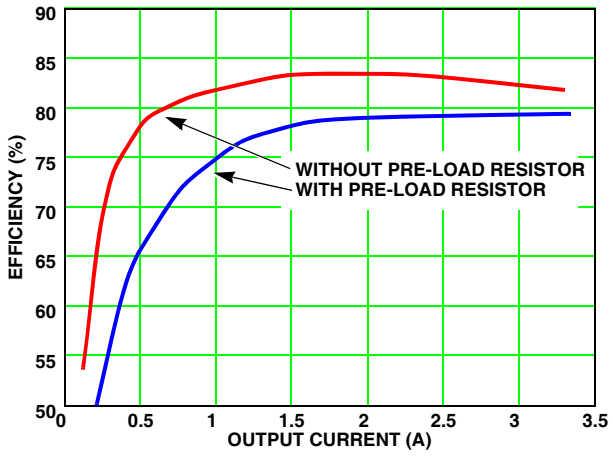


FIGURE 7. TYPICAL EFFICIENCY CONDITION: V_{IN} = 48V

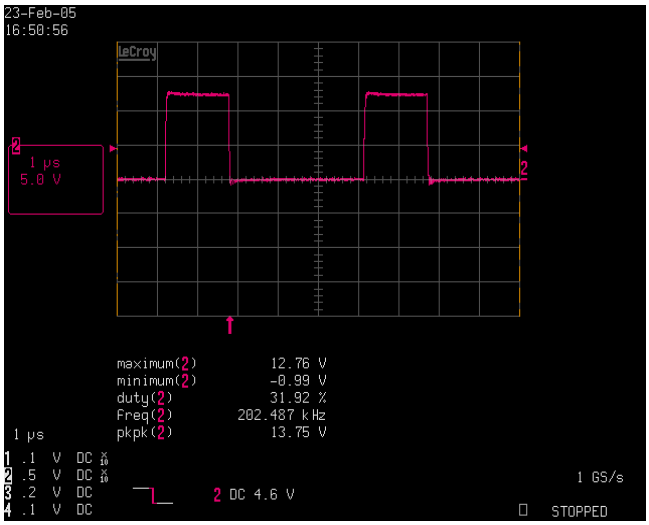


FIGURE 8. PRIMARY GATE DRIVE - Vgs of Q2 CONDITION: V_{IN} = 48V, I_{OUT} = 3.1A

The primary FET gate waveform is shown in Figure 8. Since cross-conduction between the primary and secondary is not an issue here, a small gate resistor was sufficient. Adding a gate resistor helps in reducing the turn-on spikes, as well as damping oscillations of the parasitic tank circuit between the transformer's leakage inductance and the FET capacitance.

Load regulation is shown in Figure 9. As discussed under "Rectification", the regulation is loose as compared to the synchronous rectified version. However, in most applications, very tight regulation is not a requirement.

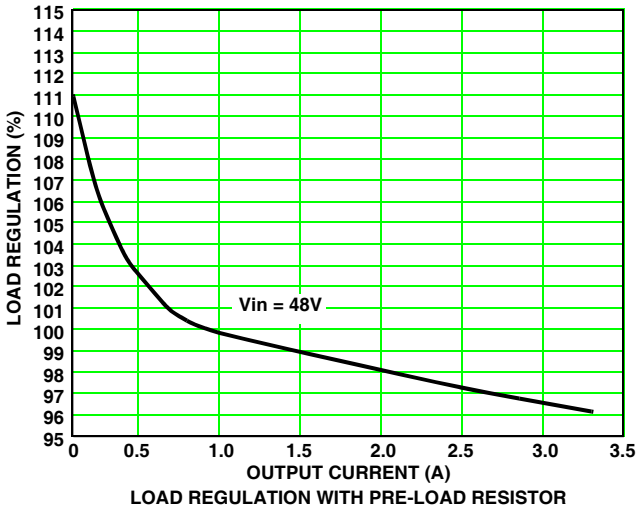


FIGURE 9. LOAD REGULATION

The output voltage ripple and noise are shown in Figure 10.

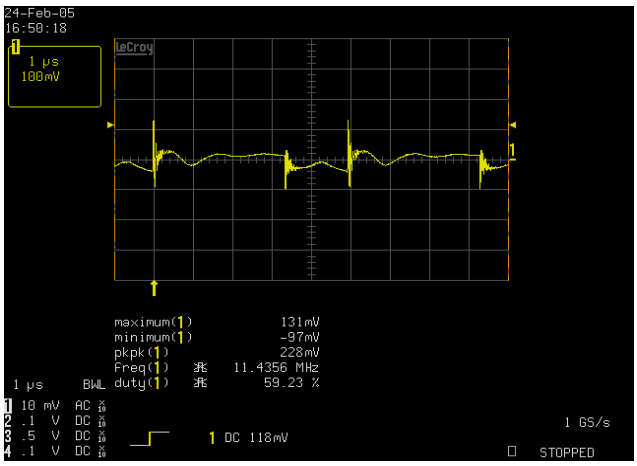


FIGURE 10. OUTPUT RIPPLE AND NOISE - 20MHz BW CONDITION: V_{IN} = 48V, I_{OUT} = 3.1A

Summary

Using a high performance, low-cost PWM controller with a low pin-count, outstanding performance has been achieved, while keeping the cost to a minimum. The schematic and BOM for both the versions are listed below. Other output voltage versions are available upon request. Please contact our Technical Support Center for custom output voltage requirements. They can be reached through Intersil's website at http://www.intersil.com or via phone at 1-888-INTERSIL.

Test Procedure

Testing the Evaluation Board

- Connect the 3.3V load between the A3 (positive) and A4 (negative) terminals.
- Plug the cable coming from the PSE, carrying the input voltage for the PD, into the Ethernet Jack J1.
- Measurements can be made on the 3.3V rail between pins A3 and A4. For ripple and noise measurements, scope probes with short ground leads must be used.
- Test Point A5 has been provided as the ground reference of the primary circuit before the series-pass FET, Q1 is turned on.
- In case of a Gigabit Network, T4 (included as part of the Evaluation Kit) will have to be populated on the board, and T3 removed. The rest of the procedure remains identical.

Testing the Power Train

- Connect the 3.3V load between the A3 (positive) and A4 (negative) terminals.
- Connect the DC power supply to the input terminals A1 (VDC) and A2 (Ground).
- Current-limit the DC power supply to about 0.5A, and turn on the supply (36V - 57V DC).
- Measurements can be made on the 3.3V rail between pins A3 and A4. For ripple and noise measurements, scope probes with short ground leads must be used.
- Test Point A5 has been provided as the ground reference of the primary circuit before the series-pass FET, Q1 is turned on.

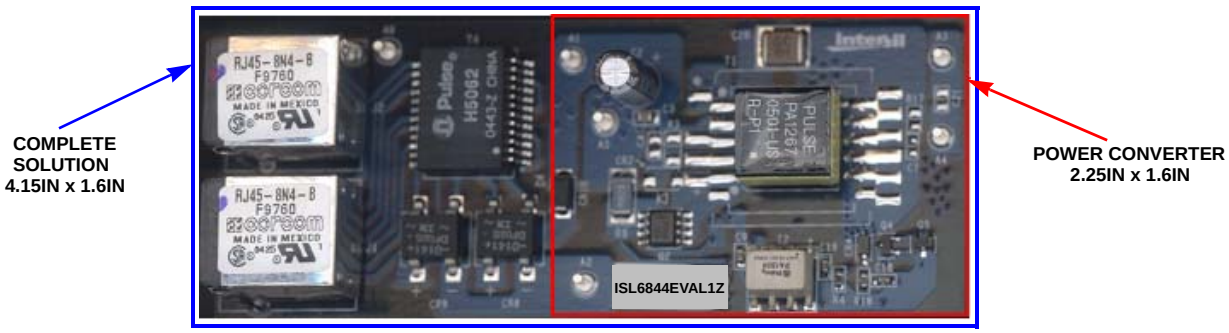


FIGURE 11. ISL6844EVAL1Z BOARD

Circuit Elements

Signature Elements – R1, C1

Input Filtering Capacitance – C2, C3

Inrush Current protection – R14, C10, Q1

Discrete UVLO – VR1, R2, VR2

Isolation Transformer – T1

Power MOSFET – Q2

Current Sense Network – R6, R7, R8, C17

Trickle-charge Bias Circuit – R13, C14

Operating Bias Circuit – CR1, R16, C5, CR7, C14

Control Circuit – U1, C13, R12, C15, R5, CR3, R20

Synchronous Rectification FET – Q3

Gate Drive Circuit for synchronous rectification – C9, T2, C19, R4, R19, Q4, Q5, CR4, R18, C18

Output Filtering – C6, C8

Feedback Network – R9, R10, R11, C11, C12

Input Connector for Power and Data - J1

Output Connector for Power and Data - J2

Input Rectifier Diodes - CR8, CR9

Ethernet Transformer (10/100 Base) - T3

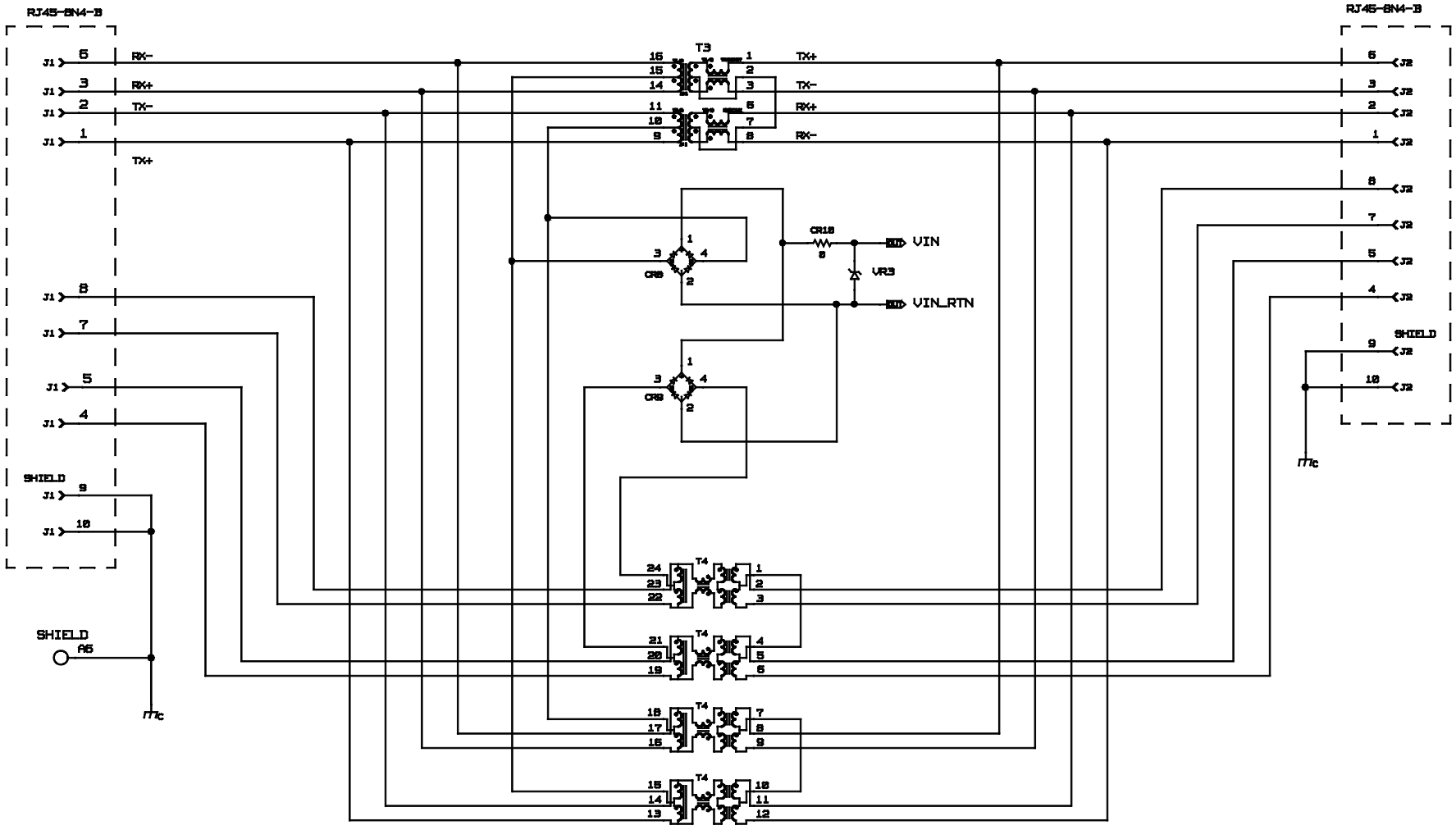
Ethernet Transformer (Gigabit Network) - T4

Transient Voltage Suppressor - VR3

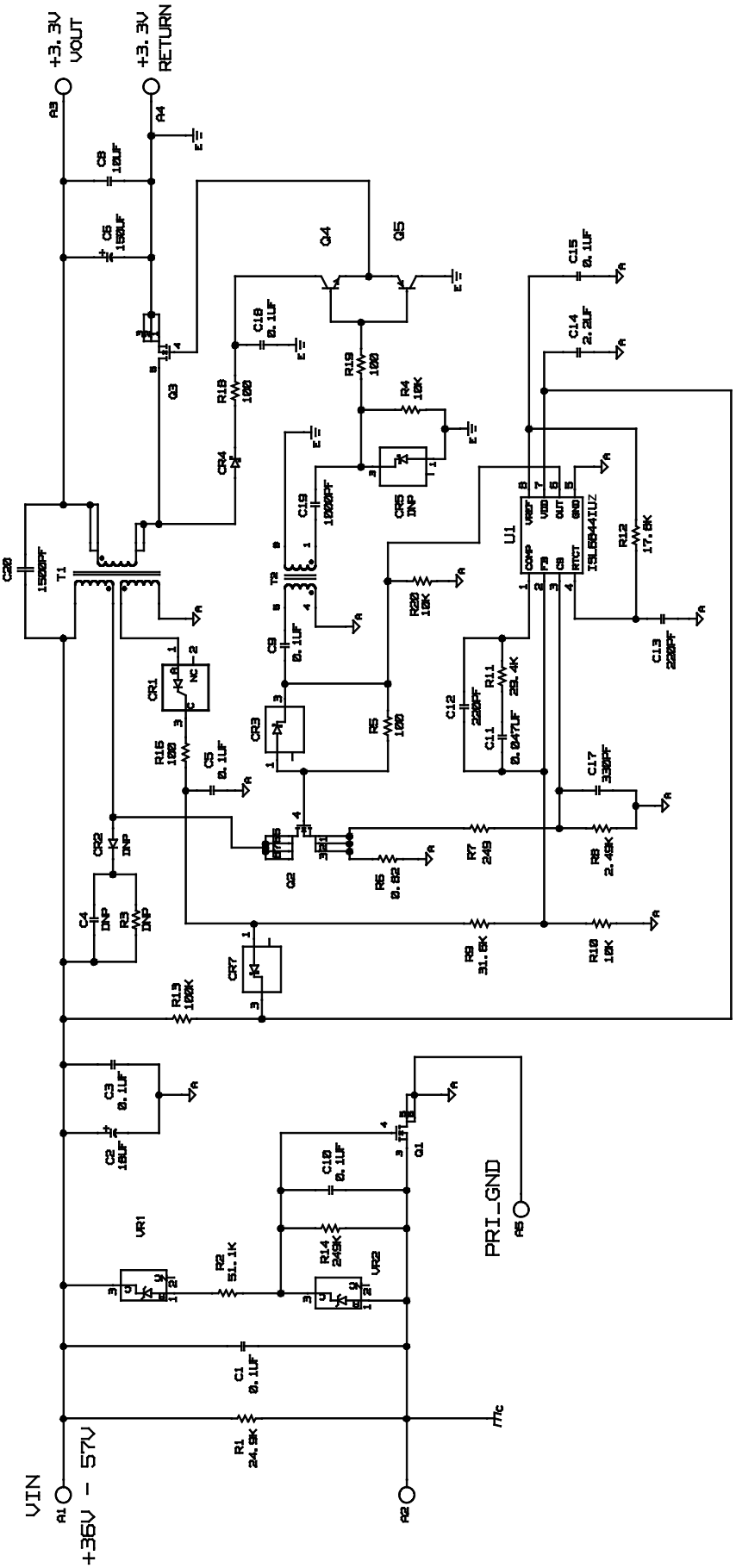
Schottky Rectifier (used in ISL6844EVAL2Z) - CR6

Safety Capacitor - C20

Front End Circuit - Identical for both ISL6844EVAL1Z and ISL6844EVAL2Z



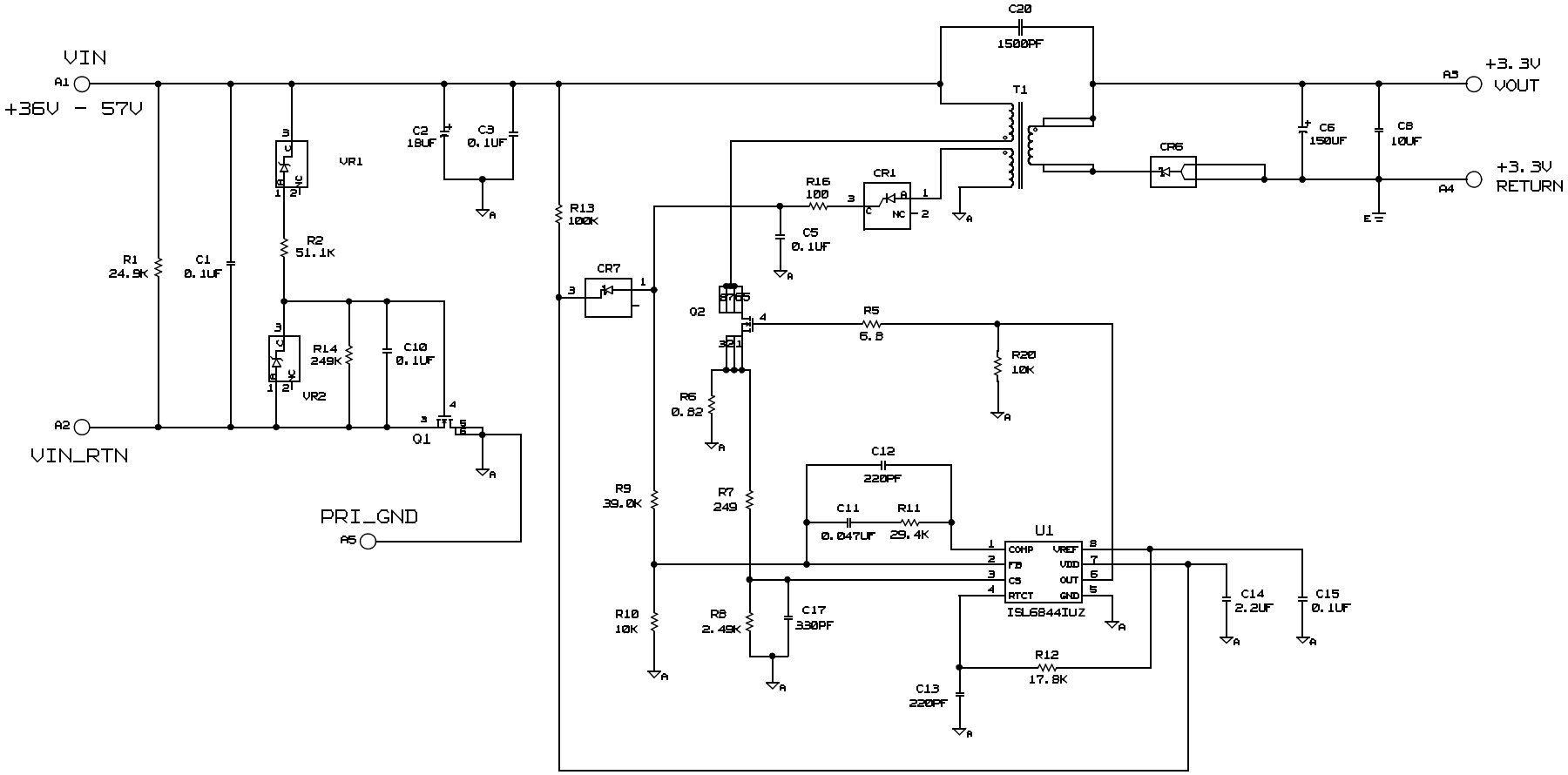
Schematic - ISL6844EVAL1Z



ISL6844EVAL1Z BOM

REF DES	QTY	PART NUMBER	DESCRIPTION	PACKAGE	VENDOR
U1	1	ISL6844IUZ	IC, PWM Controller	MSOP-8	Intersil
Q1	1	HAT2038R-EL-E	MOSFET, N-channel, 60V, 0.058Ω, 5A	SOP-8	Renesas
Q2	1	HAT2088R-EL-E	MOSFET, N-channel, 200V, 0.35Ω, 2A	SOP-8	Renesas
Q3	1	HAT2168H-EL-E	MOSFET, N-channel, 30V, 0.006Ω, 30A	LFPAK	Renesas
Q4	1	PBSS4240T	Transistor, NPN	SOT-23	Philips
Q5	1	PBSS5240T	Transistor, PNP	SOT-23	Philips
VR1	1	MMBZ5255B-7-F	Zener, 28V, 350mW	SOT-23	Diodes Inc.
VR2	1	MMBZ5240B-7-F	Zener, 10V, 350mW	SOT-23	Diodes Inc.
VR3	1	SMAJ58A	TVS, 58V, 400W	SMA	Diodes Inc.
CR1	1	BAS21	Diode, Switching	SOT-23	Diodes Inc.
CR3, CR7	2	BAT54	Diode, Rectifying	SOT-23	Diodes Inc.
CR4	1	B0540W-7-F	Diode, Schottky	SOD123	Diodes Inc.
CR8, CR9	2	DF02S	Diode-Bridge Rectifier, SMD, 200V, 1A	SM	Diodes Inc.
T1	1	PA1267NL	Transformer, Custom	EP13	Pulse
		Alternate source			Co-ev, Inc.
T2	1	PA1324NL	Gate Drive Transformer	SM	Pulse
T3	1	HX2260NL	Ethernet Transformer	SM	Pulse
C1, C3	2	C2012X7R2A104K	Cap, ceramic, X7R, 0.1µF, 10%, 100V	SM_0805	TDK
C2	1	UPW2A180MED	Cap, alum. Elec., 18µF, 20%, 100V	6.3 x 15	Nichicon
C5, C9, C10, C15, C18	5	C1608X7R1E104K	Cap, ceramic, X7R, 0.1µF, 10%, 25V	SM_0603	TDK
C6	1	EEF-SD0G151R	Cap, polymer, 150µF, 20%, 4V	7.3 x 4.3	Panasonic
C8	1	C2012X7R1A106K	Cap, ceramic, X7R, 10µF, 10%, 6.3V	SM_0805	TDK
C11	1	C1608X7R1H473K	Cap, ceramic, X7R, 0.047µF, 10%, 25V	SM_0603	TDK
C12, C13	2	C1608COG1H221J	Cap, ceramic, COG, 220pF, ± 0.5pF, 50V	SM_0603	TDK
C14	1	C2012X7R1C225K	Cap, ceramic, X7R, 2.2µF, 10%, 16V	SM_0805	TDK
C17	1	C1608COG1H331J	Cap, ceramic, COG, 330pF, 5%, 50V	SM_0603	TDK
C19	1	C1608X7R1H102K	Cap, ceramic, X7R, 1000pF, 10%, 50V	SM_0603	TDK
C20	1	GA355DR7GC152KY02L/ GA352QR7GR152KW01F	Cap, ceramic, Y-2, 1500pF, 20%, 250VAC	SM_2220	Murata
R1	1		Resistor, 24.9kΩ, 1%, 1/16W	SM_0603	Generic
R2	1		Resistor, 51.1kΩ, 1%, 1/16W	SM_0603	Generic
R4, R10, R20	3		Resistor, 10kΩ, 1%, 1/16W	SM_0603	Generic
R5, R16, R18	3		Resistor, 100Ω, 1%, 1/16W	SM_0603	Generic
R6	1		Resistor, 0.82Ω, 1%, 1/2W	SM_2512	IRC/Koa Speer
R7	1		Resistor, 249Ω, 1%, 1/16W	SM_0603	Generic
R8	1		Resistor, 2.49kΩ, 1%, 1/16W	SM_0603	Generic
R9	1		Resistor, 31.6kΩ, 1%, 1/16W	SM_0603	Generic
R11	1		Resistor, 29.4kΩ, 1%, 1/16W	SM_0603	Generic
R12	1		Resistor, 17.8kΩ, 1%, 1/16W	SM_0603	Generic
R13	1		Resistor, 100kΩ, 1%, 1/16W	SM_0603	Generic
R14	1		Resistor, 249kΩ, 1%, 1/16W	SM_0603	Generic
R19	1		Resistor, 100Ω, 1%, 1/10W	SM_0805	Generic

Schematic - ISL6844EVAL2Z



ISL6844EVAL2Z BOM

REF DES	QTY	PART NUMBER	DESCRIPTION	PACKAGE	VENDOR
U1	1	ISL6844IUZ	IC, PWM Controller	MSOP-8	Intersil
Q1	1	HAT2038R-EL-E	MOSFET, N-channel, 60V, 0.058Ω, 5A	SOP-8	Renesas
Q2	1	HAT2088R-EL-E	MOSFET, N-channel, 200V, 0.35Ω, 2A	SOP-8	Renesas
VR1	1	MMBZ5255B-7-F	Zener, 28V, 350mW	SOT-23	Diodes Inc.
VR2	1	MMBZ5240B-7-F	Zener, 10V, 350mW	SOT-23	Diodes Inc.
VR3	1	SMAJ58A	TVS, 58V, 400W	SMA	Diodes Inc.
CR1	1	BAS21	Diode, Switching	SOT-23	Diodes Inc.
CR6	1	PDS1040-13	Diode, Schottky, 40V, 10A	DPAK	Diodes Inc.
CR7	1	BAT54	Diode, Rectifying	SOT-23	Diodes Inc.
CR8, CR9	2	DF02S	Diode-Bridge Rectifier, SMD, 200V, 1A	SM	Diodes Inc.
T1	1	PA1267NL	Transformer, Custom	EP13	Pulse
		Alternate source			Co-ev, Inc.
T3	1	HX2260NL	Ethernet Transformer	SM	Pulse
C1, C3	2	C2012X7R2A104K	Capacitor, ceramic, X7R, 0.1µF, 10%, 100V	SM_0805	TDK
C2	1	UPW2A180MED	Cap, alum. Elec., 18µF, 20%, 100V	6.3 x 15	Nichicon
C5, C10, C15	3	C1608X7R1E104K	Capacitor, ceramic, X7R, 0.1µF, 10%, 25V	SM_0805	TDK
C6	1	EEF-SD0G151R	Cap, polymer, 150µF, 20%, 4V	7.3 x 4.3	Panasonic
C8	1	C2012X7R1A106K	Cap, ceramic, 10µF, X7R, 10%, 6.3V	SM_0805	TDK
C11	1	C1608X7R1H473K	Cap, ceramic, X7R, 0.047µF, 10%, 25V	SM_0603	TDK
C12, C13	2	C1608COG1H221J	Cap, ceramic, COG, 220pF, ±0.5pF, 50V	SM_0603	TDK
C14	1	C2012X7R1C225K	Cap, ceramic, X7R, 2.2µF, 10%, 16V	SM_0805	TDK
C17	1	C1608COG1H331J	Cap, ceramic, COG, 330pF, 5%, 50V	SM_0603	TDK
C20	1	GA355DR7GC152KY02L/ GA352QR7GR152KW01F	Cap, ceramic, Y-2, 1500pF, 20%, 250VAC	SM_2220	Murata
R1	1		Resistor, 24.9kΩ, 1%, 1/16W	SM_0603	Generic
R2	1		Resistor, 51.1kΩ, 1%, 1/16W	SM_0603	Generic
R5	1		Resistor, 6.8Ω, 5%, 1/10W	SM_0603	Generic
R6	1		Resistor, 0.82Ω, 1%, 1W	SM_2512	IRC/Koa Speer
R7	1		Resistor, 249Ω, 1%, 1/16W	SM_0603	Generic
R8	1		Resistor, 2.49kΩ, 1%, 1/16W	SM_0603	Generic
R9	1		Resistor, 39.0kΩ, 1%, 1/16W	SM_0603	Generic
R10, R20	2		Resistor, 10kΩ, 1%, 1/16W	SM_0603	Generic
R11	1		Resistor, 29.4kΩ, 1%, 1/16W	SM_0603	Generic
R12	1		Resistor, 17.8kΩ, 1%, 1/16W	SM_0603	Generic
R13	1		Resistor, 100kΩ, 1%, 1/16W	SM_0603	Generic
R14	1		Resistor, 249kΩ, 1%, 1/16W	SM_0603	Generic
R16	1		Resistor, 100Ω, 1%, 1/16W	SM_0603	Generic